



Level-0 MDT Trigger WBS: 6.8.2.2

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P6 Task Scrubbing June 17, 2016



Overview

√ Justification of task durations:

- Group experience in NSW trigger simulation
- Looked at comparable project: NSW MM Trigger Processor
- Advice from experienced colleagues (physics & EE)
- Task length do take into account %FTE available

√ Spreadsheet color coding

- ATLAS milestones (taken from the scopping document)
- Project & external dependencies milestones
- Procurement of "large" items
 - Small material purchase used Yes in material column



Tasks layout

- √ Trigger algorithm tasks in parallel to firmware implementation
 - Algorithm development performed Research Associate (Kostas Ntekas)
 - Firmware by EE-I
- √ Firmware testing tasks run in parallel to EE firmware/AMC design
 - Testing will be done by K. Ntekas (up to 3/19), EE students (& off project personal). EE's supervise.

	Name	Duration	Start	Finish	t Quarter 2017			2nd Quarter 2017			3rd Quar	ter 2017		4th Quarter 2017			1st Quarter 2018			2nd Quarter 2018	
					Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May
24 🍫	Evaluation board firmware v1 design - barrel single region	30 d	2/1/17	3/14/17	•		— i														
25 %	Evaluation board firmware v1 simulation - barrel single region	30 d	3/15/17	4/25/17			4														
26 %	Procurement evaluation board and bench test equipment	10 d	4/12/17	4/25/17				P													
27 %	Evaluation board firmware v1 implementation - barrel single region	10 d	4/26/17	5/9/17				4													
28 %	Evaluation board firmware v1 validation - barrel single region	30 d	5/9/17	6/20/17					_	_											
31 🍫	Evaluation board latency v1 estimation - barrel single region	20 d	6/20/17	7/18/17																	
34 🍫	Evaluation board firmware v1 design - barrel multiple region	20 d	5/9/17	6/6/17					-												
35 🍫	Evaluation board firmware v1 simulation - barrel multiple region	20 d	6/7/17	7/4/17						4											
36 %	Evaluation board firmware v1 implementation - barrel multiple region	10 d	7/5/17	7/18/17						l	•										
37 %	Evaluation board firmware v1 validation - barrel multiple region	30 d	7/18/17	8/29/17							-)								
40 %	Evaluation board latency v1 estimation - barrel multiple region	20 d	8/29/17	9/26/17								L,									
43 %	Evaluation board firmware v1 design - endcap single and multiple region	25 d	7/18/17	8/22/17							4										
44 %	Evaluation board firmware v1 simulation - endcap single and multiple region	25 d	8/22/17	9/26/17								4	_								
45 *	Evaluation board firmware v1 implementation - endcap single and multiple region	10 d	9/26/17	10/10/1									L,								
46 %	Evaluation board firmware v1 validation - endcap single and multiple region	30 d	10/10/17	11/21/1										-	_						
49 %	Evaluation board latency v1 estimation - endcap single and multiple region	20 d	11/21/17	12/19/1										Γ		_	1				
52 *	Milestone: Firmware v1 implementation and test on evaluation board complete		12/19/17													**	12/19/17				
53 *	Evaluation board firmware design - v2	40 d	10/10/17	12/5/17										4		<u></u>					
54 %	Evaluation board firmware simulation - v2	40 d	12/5/17	1/30/18												-		Ь			
55 *	Evaluation board firmware implementation - v2	10 d	1/30/18	2/13/18													L,	_			
56 %	Evaluation board firmware v2 validation and latency estimation	40 d	2/13/18	4/10/18														-		Т	
59 2	Milestone: Firmware v2 implementation and test on evaluation board complete		4/10/18																	0 4 /1	0/18